REMARKS

Claims 1, 2, 4-6, 9, 13, 14, 20, 21, 23-27, 31, 32, 34 and 35 were rejected under 35 U.S.C. 102(b) as being anticipated by Forbes; claims 3, 7, 8, 22, 33 and 37 were rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes; claims 10-12, 28 and 36 were rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes in view of Wolf; claims 15-17, 29, 30, 38 and 39 were rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes in view of Wolf and Keshavarzi; and claims 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes, Wolf and Keshavarzi as applied to claim 15, and further in view of De.

In rejecting independent claims 1 and 20 of the instant invention the examiner describes the Forbes et al. patent as having a first power supply line electrically coupled to the first active region and providing a first supply voltage to the first active region (word line, coupled to the active region of the FET, the word line WL (cf. Figure 1 and column 4, lines 53-67) governing the gate voltage and thus determining the channel conductivity, the channel residing in the active region of the FET by setting the voltage across the channel). To determine what is meant by active region in claims 1 and 20 the examiner is directed to Figure 2 and page 9, lines 30-33, page 10, lines 1-4, page 24, line 6-8, and page 24, lines 13-15. In Figure 2 the low supply line 42 is shown connected to the active region source/drain 64 of the n-channel transistor 60 and the high supply line 44 is shown connected to the active region drain/source 72 of the p-channel transistor 62. This is described on page 13 of the instant disclosure. On page 9 of the instant disclosure the word line and the bit lines are distinguished. Also on page 9 lines 30 to 33 the active source region of the n-channel transistor is described. On the following page 10 the active source region of the p-channel transistor is described. This description is reiterated on page 24 where it is stated that each transistor has an active source region and an active drain region. Clearly then the words "active region" as used in claims 1 and 20 refer to the source/drain bit line region of the transistors comprising the cell.

For a 102 reference to be valid each and every element of the claimed invention must be found in the claims. Claim 1 and 20 of the instant invention claim a structure where a voltage is applied to the active region source and/or drain of the transistor. This feature is not found in the Forbes et al. reference where, in the examiners own words, a connection to the transistor gate (i.e. word line) is taught and disclosed. As such the Forbes et al. patent is not a valid 102 reference and claims 1 and 20 are allowable over the cited art. Claims 2-19 are dependent on claim 1 and contain all the limitations contained in claim 1. The Forbes patent neither teaches nor anticipates the limitations in claim 1 and therefore dependent claims 2-19 are allowable over the Forbes et al. patent under 102 or 103. Claims 21-30 are dependent on claim 20 and contain all the limitations contained in claim 20. The Forbes patent neither teaches nor anticipates the limitations in claim 20 and therefore dependent claims 2-19 are allowable over the Forbes et al. patent under either 102 or 103.

Claim 31 has been amended to include the limitation of the strap cell body region comprising a well region. Clearly there is no strap cell with a well body region in the Forbes et al. patent and therefore amended claim 31 is allowable over the Forbes et al. patent. Dependent claims 32-35 and 37 all contain the limitations of amended claim 31 and are also allowable over the Forbes et al. patent.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made."**

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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Version with Markings to Show Changes Made

31. (Amended) A memory array strap cell comprising:

a first strap cell body region comprising a well region and operable to be coupled to a first bit cell body region of a bit cell comprising a first transistor including a first active region disposed in the first bit cell body region; and

a first conductive contact coupled to the first strap cell body region;

wherein the strap cell is operable to communicate a first offset voltage potential from a first offset supply line to the first bit cell body region via the first conductive contact and the first strap cell body region; and

wherein the first offset voltage potential is operable to be different from a first supply voltage potential received by the first active region from a first power supply line.